Abstract

A processor having a register renaming structure and method is disclosed to recover a free list. The processor includes a physical register file including physical registers. The processor also includes a decoder to decode an instruction to indicate a destination logical register. The processor also includes a register allocation table to map the destination logical register to an allocated physical register. The processor also includes an active list that includes an old field and a new field. The old field includes at least one evicted physical register from the register alias table. The new field includes the allocated physical register. The processor also includes the free list of unallocated physical registers reclaimed from the active list.